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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,143	03/24/2004	Peter Gregorius	1406/144/2	5272

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/808,143	GREGORIUS ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) 1-12 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 13-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 June 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group I, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on October 5, 2005. Applicant is requested to cancel claims 1-12 in the next response.

2. Claims 13-24 are present for examination.

Claim Objections

3. Claim 20 is objected to because of the following informalities. Appropriate correction is required.

In claim 20, line 2, should "(1)" be deleted?

Claim Rejections - 35 USC § 112

4. Claims 13-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, line 2, does applicant mean to say --via a plurality of signal lines-- instead of "via a signal line"?

Claim 16 recites the limitation "the control logic" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 22 recites the limitation "the control logic" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 23 recites the limitation "the delay compensation unit" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13, 15, 17-21, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kliza et al. (U.S. Patent No. 5,852,640, referring hereafter as Kliza).

Regarding claim 13, Kliza discloses, in FIG. 10, a memory buffer (clock source 111 and skew minimizing phase shift blocks 91-94) for a memory module board (memory modules are often implemented on printed circuit board or memory module board) which is connected via a plurality of signal lines (transmission lines connecting to digital subsystems 121-124) to a plurality of memory modules (digital subsystems 121-124) mounted on said memory module board having different signal line lengths, wherein the memory buffer comprises for each signal line a corresponding integration circuit (which can comprise both computational circuit 117b-120b and time measurement unit 117a-120a, or computational circuit 117b-120b alone) for integrating the transmission time of a measurement pulse (clock pulse generated by clock source 111) transmitted via said signal line between said memory buffer and a memory module connected to said signal line.

Regarding claim 15, Kliza discloses the signal line is a transmission line. Transmission line is defined as a conducting line used to transmitted signal energy between two points,

therefore, transmission line in Kliza can be command line, address line, or data line because command, address, and data are all signal being transferred in form of signal energy.

Regarding claim 17, Kliza further discloses wherein the memory buffer comprises a measurement pulse detector (time measurement unit 117a-120a) which detects a measurement pulse received via said signal line.

Regarding claim 18, Kliza discloses wherein the integration circuit (computational circuit 117b-120b) of a signal line is connected to a corresponding measurement pulse detector (time measurement unit 117a-120a) of said signal line to receive a stop signal when a measurement pulse is detected by said pulse detector (see FIG. 18 for detail)

Regarding claim 19, Kliza discloses wherein the memory buffer comprises a signal line delay memory (non-volatile memory 149 in all computational circuits 117b-120b) for storing the integrated values of all integration circuits provided within said memory buffer as delay times of the corresponding signal lines.

Regarding claim 20, Kliza discloses wherein the memory buffer comprises a delay compensation unit (adjustable delay elements AD 91-94) which compensates the delay times of the signal lines depending on the delay times stored in said signal line delay memory to provide an equal standard time delay for all signal lines of said memory buffer (see FIG. 14 for equal standard time delay for signal lines DS1-DS4).

Regarding claim 21, Kliza also discloses, in FIG. 13, the integration circuits are supplied with a phase adjusted clock signal (output from phase locked loop 141) generated by a clock phase generator (phase locked loop 141) to integrate time fractions of a clock period of a clock

signal (output from clock source 111) generated by a clock signal generator (clock source 111) provided within said memory buffer.

Regarding claim 24, Kliza implicitly discloses the digital subsystems can be any types of memory, which store data in binary/digital format, such as DRAM, SRAM, EEPROM, flash memory, etc.

Allowable Subject Matter

7. Claims 14, 16, 22-23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matters:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kliza, Zielbauer, Braun et al., and Zumkehr, taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

As in claim 14: wherein the memory buffer comprises a control logic which sense a measurement start command to the memory modules via a control line of a command and address bus; or

As in claim 16, wherein each integration circuit is connected to the control logic to receive a start signal when the measurement start command is sent to the memory modules; or

As in claim 22, wherein the memory buffer comprises a measurement pulse generator which transmits a measurement pulse via the signal line when the control logic sends a measurement start command to the memory modules; or

As in claim 23, wherein the delay compensation unit is connected via signal lines to a microcontroller mounted on a motherboard.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 4, 2006

VanThu Nguyen
Primary Examiner
Art Unit 2824